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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

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ELLIOTT IV, BENJAMIN H	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,154	HILL ET AL.	
	Examiner	Art Unit	
	BENJAMIN ELLIOTT	4144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *53-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *53-57,60-68,70 and 72-80* is/are rejected.

7)☒ Claim(s) *58,59,69 and 71* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/23/2006, 1/04/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 53-80 have been examined and are pending.

Information Disclosure Statement

2. Initialed and dated copies of Applicant's IDS form 1449 submitted on 3/23/2006 and 1/04/2007 are attached to the instant office action.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 78 and 79 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. A "suite of computer programs" as described is non-statutory. The "programs" are not tied to tangible computer storage medium executed by a machine or processor to provide necessary functional and structural interrelationship and to produce useful, concrete and tangible result(s).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 53-57, and 60-80 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by US Patent Publication 2002/0039364 A1 by Kamiya et al (hereinafter "Kamiya").

As per Claim 53, Kamiya discloses **a matching method for a switch arrangement comprising number N of first elements , each first element arranged to at least provide ingress to the switch arrangement, each of the first N elements comprising a number L1 of first sub-elements** ([0014]. The invention allows for a scheduler to schedule packets for forwarding. "N" designates the input ports. "N" is equally divided into "M" input groups.), **the switch arrangement having a number ML2 of second sub-elements arranged to at least provide egress from said switch arrangement** ([0014]. "N" also designates the output ports. The output ports are equally divided into "M" output groups. For further clarification, "N" of applicant's design corresponds to "N" of Kamiya; "L1" of applicant's design corresponds to "M" of Kamiya (input sub-element); "ML2" of applicant's design corresponds to "M" of Kamiya (output sub-element).), **and wherein each of the first L1 sub- elements is capable of conveying a service request for at least one of said second sub- elements ML2** ([0015]. The invention allows for storing packet forwarding requests in an MxM size matrix. The requests correspond from a set in the input group of input ports to a set in the output group of the output port.), wherein the ML2 sub-elements are grouped into M aggregations of L2 sub-elements ([0014]. "N" also designates the output ports. The output ports are equally divided into "M" output ports.), **and the method comprises:**

firstly, for every one of the N first elements, aggregating service requests from all L1 first sub-elements to each of the M aggregations of L2 second sub-elements and secondly, resolving contention for said service requests from all N first elements to one or more of said M aggregations of L2 second sub-elements (Figure 3, [0041-0042]. The matrix is divided into an MxM style matrix which, in a particular embodiment of the invention, where a scheduling module S(i, j) corresponds to a combination of i-th input group and j-th output group. The scheduling module makes a two-dimensional reservation of input and output ports based on the requests to avoid collisions with other scheduling modules.),

and thirdly, for each first element, resolving contention between the L1 sub-elements and said M aggregations of L2 second sub-elements (Figure 3, [0041-0042]. The matrix is divided into an MxM style matrix which, in a particular embodiment of the invention, where a scheduling module S(i, j) corresponds to a combination of i-th input group and j-th output group. The scheduling module makes a two-dimensional reservation of input and output ports based on the requests to avoid collisions with other scheduling modules. All collisions are avoided between any scheduling module based on the embodiment of the invention.).

As per Claim 54, Kamiya **discloses a matching method as claimed in claim 53, wherein the matching method comprises the following steps:**

performing a first matching across the switch fabric for each of the plurality of N input elements and the ML2 sub-elements by performing the steps of:

summing a number of requests from each of the L1 sub-elements of the input

element (Figure 5a, Figure 5b, [0046]. The groups allocated to the input and output ports are arranged in a matrix. A scheduling module contains elements that are allotted either a logical "0" or "1". That indicates the presence or absence of a packet forwarding request.);

generating a first N x ML2 request matrix matching the first request matrix to generate a first matrix of accepted requests ([0047]. The scheduling module stores a 4x4 matrix that contains input ports in the vertical direction and output ports in the horizontal direction.);

and performing a second matching across the switch fabric for each of the N input elements by performing the steps of:

generating N asymmetric second L1 x ML2 matrices, one for each of the N input elements (Figure 5a. In the matrix of scheduling modules, there are many 4x4 matrices. Each matrix contains vertical elements of 4 (inputs), and horizontal elements of 4 (outputs). The matrices are asymmetric in the fact they contain only 4x4 inputs and outputs.);

and matching each of the N asymmetric second matrices to generate N second matrices of accepted requests ([0048]. As an example, when a packet is received at an input port to be forwarded to an output port, a request is sent to a scheduler. The request enters the module, and changes from a logical "0" to a "1" showing acceptance.);

and generating a NL1 x ML2 matrix of accepted requests from the first N x ML2 matrix of accepted requests and the N second L1x ML2 accepted request

matrices (Figure 5a, [0048]. Accepted requests (logical "1s") create a 4x4 matrix of the invention design. As described earlier, the input ports make-up the vertical elements, and the output ports make-up the horizontal elements. Each module contains an increasing sub-element (with regards to this invention, the sub-elements are "M", designated for either input ports or output ports). [0040]. For example, a scheduling module, S(M,M), contains a sub-element for the input and a sub-element for the output.).

As per Claim 55, Kamiya discloses **a matching method as claimed in claim 54, wherein the NL1 x ML2 matrix of requests is symmetric** ([0046]. Each scheduling module is stored in 4x4 matrix.).

As per Claim 56, Kamiya discloses **a matching method as claimed in claim 54, wherein L1 is equal to L2 and N is equal to M** (Figure 5a. As per applicant:

L1 = input sub-element,

L2 = output sub-element,

N = input port (ingress), and

M = output port (egress).

By way of example, with regards to Figure 5a of Kamiya, scheduling module S6 shows the vertical and horizontal elements match (5-8 and 5-8). With regards to N is equal to M, each column and row designates a number (i.e. 261, 262, 266, etc.). These numbers correspond to the input ports and output ports. Thus row marked 265 can share M and N.).

As per Claim 57, Kamiya discloses **a matching method as claimed in 54, wherein a said sub-element comprise one of the following:**

a port of a switch ([0014]. Packet connections of input ports are forwarded to output ports of a crosspoint switch.);

a port of a switching network;

a wavelength channel in an optical network;

a node in an optical ring network;

a terminal in an un-amplified passive optical network;

a terminal in an amplified passive optical network.

As per Claim 60, Kamiya discloses **a matching method as claimed in claim 53, wherein the ML2 output sub-elements are grouped first into M groups of L2 sub-elements** ([0014]. "N" also designates the output ports. The output ports are equally divided into "M" output groups.), **and matching is performed first at the group level between the N groups of L1 input sub-elements and the M groups of L2 output sub-elements, and then, for each of the N groups of L1 input sub-elements, between the L1 individual input sub-elements and the M groups of L2 output sub-elements** ([0040]. For example, a scheduling module, S(M,M), contains a sub-element for the input and a sub-element for the output. The first "M" in the parentheses corresponds to the input port sub-element or group member, whereas the second "M" corresponds to the output port sub-element or group. [0017]. The invention allows for grouping possible combinations of the N input ports and the N output ports into MxM

groups, wherein the N input ports are equally divided into M groups and the N output ports are equally divided into M groups.).

As per Claim 62, Kamiya discloses **a matching method as claimed in claim 53, wherein the step of resolving contention between the L1 sub-elements and said second ML2 sub-elements is performed in parallel for each said first element** (Figure 3, [0041-0042]. The matrix is divided into an MxM style matrix which, in a particular embodiment of the invention, where a scheduling module S(i, j) corresponds to a combination of i-th input group and j-th output group. The scheduling module makes a two-dimensional reservation of input and output ports based on the requests to avoid collisions with other scheduling modules. All collisions are avoided between any scheduling modules based on the embodiment of the invention. [0015]. The scheduling method of the invention allows for storing logical queues associated with inputs and outputs.).

As per Claim 63, Kamiya discloses **a matching method as claimed in claim 60, wherein said first and second sub-elements comprise ports in the switch arrangement** ([0014]. Packet connections of input ports are forwarded to output ports of a crosspoint switch.), **said first elements comprise aggregations of said first sub-elements and said second elements comprise aggregations of said second sub-elements** ([0017]. The invention allows for grouping possible combinations of the N input ports and the N output ports into MxM groups, wherein the N input ports are equally divided into M groups and the N output ports are equally divided into M groups.).

As per Claim 64, Kamiya discloses **a matching method as claimed in claim 53, wherein said switch arrangement comprises an input queued cell switch arrangement** ([0015]. The invention allows for storing "N" logical queues for each "N" input port.), **and said service requests comprise requests for transmitting a service information rate from one of said first sub-elements to at least one of said second sub-elements** ([0006]. A bit represents a request from a corresponding input port to a corresponding output port. A diagonal arrangement of service patterns is used to provide guaranteed service.).

As per Claim 65, Kamiya discloses **a matching method as claimed in claim 53, wherein said switch arrangement comprises an input queued cell switch** ([0015]. The invention allows for storing "N" logical queues for each "N" input port.), **and said service requests comprise requests for transmitting at least one cell from one of said first sub-elements to at least one of said second sub-elements** ([0036]. The crosspoint switch performs switching of cells (fixed-length packets). [0015]. These packets are in the form of requests from input ports to corresponding output ports.).

As per Claim 80, Kamiya discloses **a scheduler for a switching arrangement, the scheduler arranged to perform a scheduling process, the scheduling process comprising:**
a matching method as claimed in claim 53; and a channel assignment process (Abstract. The invention contains a scheduler. [0002]. The scheduler allows for a pipelined scheduling method. [0014]. The scheduler assigns outputs to corresponding inputs.).

As per Claim 70, Kamiya discloses **a matching method for a multi-stage switch arrangement having a plurality of logically associated inputs and a plurality of outputs** ([0015]. The scheduling method of the invention allows for storing logical queues associated with inputs and outputs.), **wherein the matching method comprises the steps of:**

for each logical association of inputs, aggregating service requests from every one of the inputs which form said logical association ([0015]. The request are stored in a MxM matrix corresponding to input groups of input ports and output groups of output ports.);

resolving contention for said aggregated service requests between all of the logical associations to the outputs of the switch arrangement (Figure 3, [0041-0042]. The matrix is divided into an MxM style matrix which, in a particular embodiment of the invention, where a scheduling module S(i, j) corresponds to a combination of i-th input group and j-th output group. The scheduling module makes a two-dimensional reservation of input and output ports based on the requests to avoid collisions with other scheduling modules. ([0015]. The scheduling method of the invention allows for storing logical queues associated with inputs and outputs. This is the logical association with respect to the outputs.);

and repeating the above steps in the matching method within each logical association for a subset of the inputs forming each said logical association until

contention is resolved between the individual inputs of the switch arrangement and the outputs of the switch arrangement ([0043]. The reserved input port information sequentially visits each row and column in a round-robin fashion. [0042]. The reserved input and output port information is used to avoid collisions.

As per Claim 72, Kamiya discloses **a method as claimed in claim 70, wherein each step resolving contention between the outputs of the switch arrangement comprises resolving contention between a logical association of inputs and a logical association of outputs having the same number of inputs** (Figure 3, [0041-0042]. The matrix is divided into an MxM style matrix which, in a particular embodiment of the invention, where a scheduling module S(i, j) corresponds to a combination of i-th input group and j-th output group. The scheduling module makes a two-dimensional reservation of input and output ports based on the requests to avoid collisions with other scheduling modules. [0015]. The scheduling method of the invention allows for storing logical queues associated with inputs and outputs. This is the logical association with respect to the outputs and inputs. [0046]. Each scheduling module is stored in 4x4 matrix, thus the number of outputs is the same number of inputs.).

As per Claim 75, Kamiya discloses **a multi-stage switch arrangement arranged to switch time-slotted traffic segments** ([0057]. The scheduler can perform "next-stage scheduling", therefore allowing multiple stage switching.), **the switch arrangement comprising:**

a plurality of switching stages including spatial switching stage arranged to receive traffic which has been switched by at least one switching stage logically adjacent to the input of spatial switching stage ([0042]. A packet is received or transmitted between an input port and an output port in a required time field. [0041]. Scheduling modules, denoted S(i,j), wherein "i" represents an input and "j" represents an output, transfers updated input port scheduling information to adjacent scheduling modules. In terms of "logic", either a logical "1" or a logical "0" is assigned based on the information provided. [0046]. "1" or "0" denotes the presence or absence of a packet forwarding request from a corresponding input port to a corresponding output port, respectively.), **the spatial switching stage being further arranged to output to at least one switching stage logically adjacent to its output** ([0041]. The same scheduling is done in terms of the output information as well.),

each of said at least one switching stage logically adjacent to the input of the spatial switching stage comprises a plurality of input aggregation switching stages ([0041]. A scheduling module S(i,j) corresponds to a combination of i-th input group and j-th output group. This grouping of sub-elements, M, within either the input port, N, or output port, N, is aggregation.),

each aggregation switching stage being logically associated with a subset of the inputs of the switch arrangement ([0046]. "1" or "0" denotes the presence or absence of a packet forwarding request from a corresponding input port to a corresponding output port, respectively.),

each of said at least one switching stage logically adjacent to the output of the

spatial switching stage comprises a plurality of output aggregation switching stages ([0041]. Scheduling modules, denoted S(i,j), wherein "i" represents an input and "j" represents an output, transfers updated output port scheduling information to adjacent scheduling modules. [0057]. The scheduler can perform "next-stage scheduling", therefore allowing multiple stage switching.).

As per Claim 76, Kamiya discloses **a switch arrangement, the switch arrangement having number N of first elements, each first element arranged to at least provide ingress to a switch arrangement, each of the first N elements comprising a number L1 of first sub-elements** ([0014]. The invention allows for a scheduler to schedule packets for forwarding. "N" designates the input ports. "N" is equally divided into "M" input groups.), **the switch arrangement having a number ML2 of second sub-elements arranged to at least provide egress from said switch arrangement** ([0014]. "N" also designates the output ports. The output ports are equally divided into "M" output groups. For further clarification, "N" of applicant's design corresponds to "N" of Kamiya; "L1" of applicant's design corresponds to "M" of Kamiya (input sub-element); "ML2" of applicant's design corresponds to "M" of Kamiya (output sub-element).), and wherein each of the first L1 sub- elements is capable of conveying a service request for at least one of said second sub- elements ML2 ([0015]. The invention allows for storing packet forwarding requests in an MxM size matrix. The requests correspond from a set in the input group of input ports to a set in the output group of the output port.), **wherein the ML2 sub-elements are grouped into M**

aggregations of L2 sub-elements ([0014]. "N" also designates the output ports. The output ports are equally divided into "M" output ports.), **wherein said service requests are conveyed by performing a matching method which comprises:**

for each of the N first elements, aggregating service requests from all L1 first sub- elements to each of the ML2 second sub-elements, and

resolving contention for said service requests from all N first elements to one or more of said second ML2 sub-elements, and

for each of the N first elements, resolving contention between the L1 sub-elements and said second ML2 sub-elements (Figure 3, [0041-0042]. The matrix is divided into an MxM style matrix which, in a particular embodiment of the invention, where a scheduling module S(i, j) corresponds to a combination of i-th input group and j-th output group. The scheduling module makes a two-dimensional reservation of input and output ports based on the requests to avoid collisions with other scheduling modules.).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 66-68, 73-74, and 77-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Publication 2002/0039364 A1 by Kamiya et al (hereinafter "Kamiya"), and further in view of US Patent Publication 2003/0016687 by Hill (hereinafter "Hill").

As per Claim 66, Kamiya is silent on **a method as claimed in claim 53, wherein said switch arrangement comprises a circuit based switch and said service request comprises a request for at least one of the following:**
a connection in the circuit-based switch;

a wavelength channel in the circuit-base J switch

a bandwidth in the circuit-based switch;

a service information rate in the circuit-based switch;

a bit rate in the circuit-based switch.

However, Hill teaches setting up connections between input ports and output ports can be done in a circuit based switch environment ([0036]. This correlates to **a connection in the circuit based switch.**). Connection requests can be made in parallel rather than sequentially ([0041]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kamiya to include the contents of the service request to comprise a connection request taught by Hill, to reduce the number of requests to effectively group input-output pairs for faster connections ([0015]).

As per Claim 67, Kamiya is silent on **a method as claimed in claim 53, wherein the switch arrangement comprises a network, and wherein said elements comprise aggregations of network terminals or nodes and said sub-elements comprise network terminals or nodes**.

However, Hill teaches that each switch comprises a processor that is coupled to a grouping of elements. The elements are therefore matched between the first and third stages for pairing ([0041]). The processors act as network terminals or nodes of the switching network ([0044]).

Examiner maintains the motivation to combine the teachings of Kamiya and Hill as stated in Claim 66.

As per Claim 68, Kamiya is silent on **a method as claimed in claim 53, wherein the switch arrangement comprises an arrangement of inter-connectable sub-networks, where said elements comprise sub-networks and said sub-elements comprise network terminals or nodes.**

However, Hill teaches the switching arrangement can be incorporated into a switching fabric, which is an interconnection of network switches ([0067]). Also, Hill teaches that each switch comprises a processor that is coupled to a grouping of elements. The elements are therefore matched between the first and third stages for pairing ([0041]). The processors act as network terminals or nodes of the switching network ([0044]).

Examiner maintains the motivation to combine the teachings of Kamiya and Hill as stated in Claim 66.

As per Claim 73, Kamiya discloses **a matching method as claimed in claim 70, wherein said multi-stage switch arrangement comprises a plurality of switching stages** ([0057]. The scheduler can perform "next-stage scheduling", therefore allowing multiple stage switching.), **at least one switching stage comprising:**
a plurality of switches which logically associated into different sets of switches, each set of switches being logically associated with one of said logical

associations of inputs of the switch arrangement, wherein each set of logically associated switches operate only on the inputs of the switch arrangement with which they are logically associated, the switch arrangement further comprising a global spatial switching stage arranged to receive traffic derived from any of the inputs of the switch arrangement via any logically adjacent sets of said switches ([0042]. A packet is received or transmitted between an input port and an output port in a required time field. [0041]. Scheduling modules, denoted S(i,j), wherein "i" represents an input and "j" represents an output, transfers updated input port scheduling information to adjacent scheduling modules. In terms of "logic", either a logical "1" or a logical "0" is assigned based on the information provided. [0046]. "1" or "0" denotes the presence or absence of a packet forwarding request from a corresponding input port to a corresponding output port, respectively.).

Kamiya is silent on the switching stages having a plurality of switches.

However, Hill teaches that the switch of the invention's design contains a plurality of first stage switches, middle stage switches, and third stage switches.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kamiya to include multiple stage switching inside one of the stages of switching taught by Hill to reduce the number of requests to effectively group input-output pairs for faster connections ([0015]).

As per Claim 74, Kamiya discloses **a matching method as claimed in claim 70, wherein said multi-stage switch arrangement comprises a plurality of switching stages** ([0057]. The scheduler can perform "next-stage scheduling", therefore allowing

multiple stage switching.), **at least one switching stage comprising:**

a plurality of switches which logically associated into different sets of switches, each set of switches being logically associated with one of said logical associations of outputs of the switch arrangement, wherein each set of logically associated switches operate only to provide output to the outputs of the switch arrangement with which they are logically associated ([0042]. A packet is received or transmitted between an input port and an output port in a required time field. [0041]. Scheduling modules, denoted S(i,j), wherein "i" represents an input and "j" represents an output, transfers updated input port scheduling information to adjacent scheduling modules. In terms of "logic", either a logical “1” or a logical “0” is assigned based on the information provided. [0046]. “1” or "0" denotes the presence or absence of a packet forwarding request from a corresponding input port to a corresponding output port, respectively.).

Kamiya is silent on the switching stages having a plurality of switches.

However, Hill teaches that the switch of the invention's design contains a plurality of first stage switches, middle stage switches, and third stage switches.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kamiya to include multiple stage switching inside one of the stages of switching taught by Hill to reduce the number of requests to effectively group input-output pairs for faster connections ([0015]).

As per Claim 77, Kamiya is silent on **a network including a switch arrangement as claimed in claim 70.**

However, Hill teaches that each switch comprises a processor that is coupled to a grouping of elements. The elements are therefore matched between the first and third stages for pairing ([0041]). The processors act as network terminals or nodes of the switching network ([0044]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kamiya to include the contents of the service request to comprise a connection request taught by Hill, to reduce the number of requests to effectively group input-output pairs for faster connections ([0015]).

As per Claim 78, Kamiya is silent on **a suite of at least one computer programs arranged when executed to implement steps in a method according to claim 53.**

However, Hill teaches that each switch comprises a processor that is coupled to a grouping of elements. The elements are therefore matched between the first and third stages for pairing ([0041]). The processors act as network terminals or nodes of the switching network ([0044]). Figure 11 shows how memory is used to determine if an output port is free and resolve contention between the ports.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kamiya to include running a program to

implement steps of the method as described in Claim 53 taught by Hill to fully enable all steps associated with any method to be implemented by a computer.

As per Claim 79, Kamiya is silent on **a suite of at least one computer programs as claimed in claim 78, wherein at least one program is arranged to be implemented by software running on a suitable computational device.**

However, Hill teaches that each switch comprises a processor that is coupled to a grouping of elements. The elements are therefore matched between the first and third stages for pairing ([0041]). The processors act as network terminals or nodes of the switching network ([0044]). Figure 11 shows how memory is used to determine if an output port is free and resolve contention between the ports.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kamiya to include running a program to implement steps of the method as described in Claim 53 taught by Hill to fully enable all steps associated with any method to be implemented by a computer.

10. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya, and further in view of US Patent 6,643,293 B1 by Carr et al (hereinafter "Carr").

As per Claim 61, Kamiya is silent on **a method as claimed in claim 53, wherein said first sub-elements and said second sub-elements are bi-directional.**

However, Carr teaches a technique for virtual path shaping between aggregating virtual channel connections (Abstract). The combination of an egress function and an ingress function at a bi-directional port is called a virtual path termination point, or VPTP

(col. 1, lines 62-65). The system of the invention allows for end to end connections between VPTP ports (col. 5, lines 7-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kamiya to include bi-directional ports taught by Carr to translate virtual channel connections whether they are at the ingress port or the egress port. Either port could be a terminating end of the connection or channel (col. 1, lines 58-65).

Allowable Subject Matter

11. Claims 58, 59, 69, and 71 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. Prior art made of record and not relied upon include:

US Patent 7,158,512 B1 by Kamhine teaches a system and method of scheduling through a crossbar switch.

US Patent Publication 2001/0043606 A1 by Han et al teaches a cell scheduling method of a buffered switch.

US Patent 6,570,873 B1 by Isoyama teaches a method for scheduling traffic with priority.

US Patent 6,643,286 B1 by Kapadia et al teaches interconnecting switches for minimal address mapping.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN ELLIOTT whose telephone number is (571)270-7163. The examiner can normally be reached on Monday thru Thursday, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Taghi Arani can be reached on 1-571-272-3787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/B. E./
Examiner, Art Unit 4144

/Taghi T. Arani/

Supervisory Patent Examiner, Art Unit 4144